IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method for transferring data in a system including a host computer system coupled through a communication medium to a data acquisition device, the method comprising:

configuring a data acquisition device for a data input/output (I/O) operation, wherein the data acquisition device comprises a link buffer;

the host computer system preparing a plurality of transfer links, wherein each of the plurality of transfer links specifies a transfer of data between the data acquisition device and the host computer system;

transferring a first portion of the plurality of transfer links from the host computer system to a first portion of the link buffer of the data acquisition device over the communication medium;

the data acquisition device initiating the data I/O operation;

the data acquisition device executing the first portion of the plurality of transfer links from the first portion of the link buffer to transfer data between a data buffer in the data acquisition device and host memory in the host computer system; and

transferring a second portion of the plurality of transfer links from the host computer system to a second portion of the link buffer of the data acquisition device over the communication medium, wherein at least a portion of said transferring the second portion of the plurality of transfer links and at least a portion of said executing the first portion of the plurality of transfer links are performed concurrently.

2. (Previously Presented) The method of claim 1, wherein said transferring the first portion of the plurality of transfer links to the first portion of the link buffer of the data acquisition device comprises the data acquisition device fetching the first portion of the plurality of transfer links to the first portion of the link buffer of the data acquisition device.

3. (Cancelled)

4. (Currently Amended) The method of claim 1,

wherein the data acquisition device initiating the data I/O operation comprises the host computer initiating a data acquisition process on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller[[,]]; and

wherein the data acquisition device executing the first portion of the plurality of transfer links from the first portion of the link buffer comprises:

the data acquisition device acquiring data and storing the data in the data buffer; and

the DMA Controller executing the first portion of the plurality of transfer links to transfer the data over the communication medium to the host memory in the host computer.

5. (Currently Amended) The method of claim 1,

~~wherein the host computer initiating the I/O operation on the data acquisition device comprises the host computer initiating a data generation operation on the data acquisition device;~~

wherein the data acquisition device initiating the data I/O operation comprises the host computer initiating a data acquisition process on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller[[,]]; and

wherein the data acquisition device executing the first portion of the plurality of transfer links from the first portion of the ~~memory~~ link buffer comprises:

the data acquisition device notifying the DMA Controller;

the data acquisition device requesting data from the DMA Controller; and

the DMA Controller executing the first portion of the plurality of transfer links to transfer the data from the host memory [[of]] in the host computer system to the data buffer of the data acquisition device.

6. (Currently Amended) The method of claim 1, ~~the method~~ further comprising:

the data acquisition device executing the second portion of the plurality of transfer links from the second portion of the link buffer to transfer data between [[a]] the data buffer in the data acquisition device and host memory in the host computer system; and

transferring a third portion of the plurality of transfer links from the host computer system to the first portion of the link buffer of the data acquisition device over the communication medium, wherein at least a portion of said transferring the third portion of the plurality of transfer links and at least a portion of said executing the second portion of the plurality of transfer links are performed concurrently.

7. (Currently Amended) The method of claim 6,

wherein the data acquisition device alternates between executing all transfer links from the first portion of the link buffer and all transfer links from the second portion of the link buffer, while the host computer system alternates between transferring transfer links from the host computer system to the second portion of the link buffer[[,]] and transferring transfer links from the host computer system to the first portion of the link buffer, until there are no more transfer links to transfer from the host computer system.

8. (Currently Amended) The method of claim 7,

wherein each transfer link comprises at least one of a source address or a destination address, a count of a number of bytes in the transfer, and a pointer to a subsequent transfer link.

9. (Currently Amended) The method of claim 7,

wherein one or more of the plurality of transfer links comprises a self configuration link, wherein the self configuration link comprises one or more instructions to move data to, from, or between [[the]] DMA Controller registers of a DMA Controller.

10. (Currently Amended) The method of claim 9,

wherein the self configuration link is inserted at the end of the first portion of the plurality of transfer links; and

wherein[[,]] the DMA Controller executes the first portion of the plurality of transfer links on a DMA channel; [[and]]

the method further comprising:

~~wherein~~ if the DMA channel reaches the self configuration link before the host computer system has finished transferring the second portion of the plurality of transfer links to the second portion of the link buffer, the self configuration link ~~will stop~~ stopping the DMA channel to prevent data overruns.

11. (Currently Amended) The method of claim 9,

wherein the self configuration link is inserted at the end of the second portion of the plurality of transfer links; and

wherein[[,]] the DMA Controller executes the second portion of the plurality of transfer links on a DMA channel; [[and]]

the method further comprising:

~~wherein~~ if the DMA channel reaches the self configuration link before the host computer has finished transferring the third portion of the plurality of transfer links to the first portion of the link buffer, the self configuration link ~~will stop~~ stopping the DMA channel to prevent data overruns.

12. (Currently Amended) The method of claim 9,

wherein the self configuration link is inserted in the first portion of the plurality of transfer links; and

wherein[[,]] the DMA Controller executes the first portion of the plurality of transfer links on a DMA channel; [[and]]

the method further comprising:

~~wherein~~ when the DMA channel reaches the self configuration link, notifying the host computer system ~~is notified~~ to begin transferring the second portion of the plurality of transfer links to the second portion of the link buffer.

13. (Currently Amended) The method of claim 9,

wherein the self configuration link is inserted in the second portion of the plurality of transfer links; and

wherein[[,]] the DMA Controller executes the second portion of the plurality of transfer links on a DMA channel; [[and]]

the method further comprising:

~~wherein~~ when the DMA channel reaches the self configuration link, notifying the host computer system ~~is notified~~ to begin transferring the third portion of the plurality of transfer links to the first portion of the link buffer.

14. (Previously Presented) The method of claim 1,

wherein the communication medium comprises an IEEE 1394 bus, which is compliant with an IEEE 1394 protocol specification.

15. (Original) The method of claim 14,

wherein the data acquisition device comprises a PCI device,

wherein the data acquisition device further comprises a PCI/1394 translator;

the method further comprising the PCI/1394 translator translating messages between the IEEE 1394 protocol and PCI, thereby providing a mechanism for communication between the IEEE 1394 bus and the PCI device.

16. (Currently Amended) A system for transferring data over a communication medium, the system comprising:

a data acquisition device coupled to a first end of the communication medium, wherein the data acquisition device comprises a link buffer; and

a host computer system coupled to a second end of the communication medium, wherein the host computer system is operable to communicate through the communication medium to the data acquisition device;

wherein the host computer system is further operable to prepare a plurality of transfer links and transfer a first portion of the plurality of transfer links to a first portion of the link buffer of the data acquisition device ~~in a double buffered fashion~~, wherein

each of the plurality of transfer links specifies a transfer of data between the data acquisition device and the host computer system;

wherein the data acquisition device is operable to execute the first portion of the transfer links;

wherein the host computer system is further operable to transfer a second portion of the plurality of transfer links to a second portion of the link buffer of the data acquisition device; and

wherein at least a portion of said executing the first portion of the transfer links and at least a portion of said transferring the second portion of the plurality of transfer links to the second portion of the link buffer of the data acquisition device are performed concurrently.

17. (Currently Amended) The method of claim 16, wherein said host computer system being operable to transfer the first portion of the plurality of transfer links to [[a]] the first portion of link buffer of the data acquisition device comprises the data acquisition device being operable to fetch the first portion of the plurality of transfer links to the first portion of the link buffer of the data acquisition device.

18. (Cancelled)

19. (Currently Amended) The system of claim [[18]] 16,

wherein the host computer system is further operable to:

configure the data acquisition device for data input/output; and

initiate a data I/O operation on the data acquisition device, after the host computer system transfers the first portion of the plurality of transfer links to the first portion of the link buffer of the data acquisition device.

20. (Currently Amended) The method of claim 19,

wherein the host computer system being operable to initiate the data I/O operation comprises the host computer system being operable to initiate a data acquisition process on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller[[,]]; and

wherein the data acquisition device being operable to execute the first portion of the plurality of transfer links from the first portion of the link buffer comprises:

the data acquisition device being operable to acquire data and store the data in [[the]] a data buffer in the data acquisition device; and

the DMA Controller being operable to execute the first portion of the plurality of transfer links to transfer the data over the communication medium to ~~the host~~ a memory in the host computer system.

21. (Currently Amended) The system of claim 19,

wherein the host computer system being operable to initiate the I/O operation on the data acquisition device comprises the host computer system being operable to initiate a data generation operation on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller[[,]]; and

wherein the data acquisition device being operable to execute the first portion of the plurality of transfer links from the first portion of the ~~memory~~ link buffer comprises:

the data acquisition device being operable to notify the DMA Controller;

the data acquisition device being operable to request data from the DMA Controller; and

the DMA Controller being operable to execute the first portion of the plurality of transfer links to transfer the data from [[the]] a memory of the host computer system to [[the]] a data buffer of the data acquisition device.

22. (Currently Amended) The system of claim [[18]] 16, wherein the data acquisition device is further operable to execute the second portion of the plurality of transfer links from the second portion of the link buffer;

~~wherein the data acquisition device being operable to execute the plurality of transfer links from the link buffer comprises:~~

~~the host computer being operable to transfer a first plurality of transfer links to a first portion of the link buffer and a second plurality of transfer links to a second portion of the link buffer;~~

~~the data acquisition device being operable to execute the first plurality of transfer links from the first portion of the link buffer;~~

wherein the host computer system is further ~~being~~ operable to transfer a third portion of the plurality of transfer links to the first portion of the link buffer; [[and]]

wherein the data acquisition device is further ~~being~~ operable to execute the second portion of the plurality of transfer links from the second portion of the link buffer; and

wherein at least a portion of said executing the second portion of the plurality of transfer links from the second portion of the link buffer and at least a portion of said transferring the third portion of the plurality of transfer links to the first portion of the link buffer are performed concurrently.

23. (Currently Amended) The system of claim 22,

wherein the data acquisition device is further operable to alternate between executing all transfer links from the first portion of the link buffer and all transfer links from the second portion of the link buffer, while the host computer system is further operable to alternate between transferring transfer links from the host computer system to the second portion of the link buffer[[,]] and from the host computer system to the first portion of the link buffer, until there are no more transfer links to transfer from the host computer system.

24. (Currently Amended) The system of claim 16,

wherein each transfer link comprises at least one of a source address or a destination address, a count of a number of bytes in the transfer, and a pointer to a subsequent transfer link.

25. (Currently Amended) The system of claim 16,

wherein one or more of the plurality of transfer links comprises a self configuration link, wherein the self configuration link comprises one or more instructions to move data to, from, or between [[the]] DMA Channel registers of a DMA Controller.

26 . (Currently Amended) The system of claim 25,

wherein the self configuration link is inserted at the end of the first portion of the plurality of transfer links;

wherein[[,]] the DMA Controller executes the first portion of the plurality of transfer links on a DMA channel; and

wherein if the DMA channel reaches the self configuration link before the host computer system has finished transferring the second portion of the plurality of transfer links to the second portion of the link buffer, the self configuration link [[will]] stops the DMA channel to prevent data overruns.

27. (Currently Amended) The system of claim 25,

wherein the host computer system is further operable to transfer a third portion of the plurality of transfer links to the first portion of the link buffer;

wherein the self configuration link is inserted at the end of the second portion of the plurality of transfer links;

wherein, the DMA Controller executes the second portion of the plurality of transfer links on a DMA channel; and

wherein if the DMA channel reaches the self configuration link before the host computer system has finished transferring the third portion of the plurality of transfer links to the first portion of the link buffer, the self configuration link [[will]] stops the DMA channel to prevent data overruns.

28. (Currently Amended) The system of claim 25,

wherein the self configuration link is inserted in the first portion of the plurality of transfer links;

wherein[[,]] the DMA Controller is operable to execute the first portion of the plurality of transfer links on a DMA channel; and

wherein [[when]] the DMA channel is operable to notify the host computer system to begin transferring the second portion of the plurality of transfer links to the second portion of the link buffer when the DMA channel reaches the self configuration link.

29. (Currently Amended) The system of claim 25,

wherein the host computer system is further operable to transfer a third portion of the plurality of transfer links to the first portion of the link buffer;

wherein the self configuration link is inserted in the second portion of the plurality of transfer links;

wherein[[,]] the DMA Controller is operable to execute the second portion of the plurality of transfer links on a DMA channel; and

wherein [[when]] the DMA channel is operable to notify the host computer system to begin transferring the third portion of the plurality of transfer links to the first portion of the link buffer when the DMA channel reaches the self configuration transfer link.

30. (Original) The system of claim 16,

wherein the communication medium comprises an IEEE 1394 bus, which is compliant with an IEEE 1394 protocol specification.

31. (Original) The system of claim 16,

wherein the data acquisition device comprises a PCI device,

wherein the data acquisition device further comprises a PCI/1394 translator; and

wherein the PCI/1394 translator is operable to translate messages between the IEEE 1394 protocol and PCI, thereby providing a mechanism for communication between the IEEE 1394 bus and the PCI device.

32. (Previously Presented) A method for transferring data in a system including a host computer system coupled through a communication medium to a data acquisition device, the method comprising:

configuring a data acquisition device for a data input/output (I/O) operation, wherein the data acquisition device comprises a link buffer;

the host computer system preparing a linked list of transfer nodes, wherein each of the linked list of transfer nodes includes a true address of physical memory of the host computer system;

the host computer system preparing a plurality of transfer links, wherein each of the plurality of transfer links specifies a transfer node and a transfer of data between the data acquisition device and the host computer system;

the host computer system transferring the plurality of transfer links to the link buffer of the data acquisition device over the communication medium;

the data acquisition device initiating the data I/O operation; and

the data acquisition device executing the plurality of transfer links from the link buffer to transfer data between a data buffer in the data acquisition device and the physical memory of the host computer system;

wherein, for each transfer node of the linked list of transfer nodes, the true address of the transfer node corresponds to a virtual address of a buffer, wherein the buffer spans contiguous virtual addresses mapping to the physical memory of the host computer system, wherein an Nth transfer node corresponds to an Nth virtual address of the buffer.

33. (New) The method of claim 32, wherein said transferring the plurality of transfer links to the link buffer of the data acquisition device over the communication medium comprises the data acquisition device fetching the plurality of transfer links to the link buffer of the data acquisition.

34. (New) The method of claim 32,

wherein the data acquisition device initiating the data I/O operation comprises the host computer system initiating a data acquisition process on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller; and

wherein the data acquisition device executing the plurality of transfer links from the link buffer comprises:

the data acquisition device acquiring data and storing the data in the data buffer; and

the DMA Controller executing the plurality of transfer links to transfer the data over the communication medium to the physical memory of the host computer system.

35. (New) The method of claim 32,

wherein the data acquisition device initiating the data I/O operation comprises the host computer system initiating a data acquisition process on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller; and

wherein the data acquisition device executing the plurality of transfer links from the link buffer comprises:

the data acquisition device notifying the DMA Controller;

the data acquisition device requesting data from the DMA Controller; and

the DMA Controller executing the plurality of links to transfer the data from the physical memory of the host computer to the data buffer in the data acquisition device.

36. (New) The method of claim 32, further comprising:

the host computer system preparing a second linked list of transfer nodes, wherein each of the second linked list of transfer nodes includes a true address of the physical memory of the host computer system;

the host computer system preparing a second plurality of transfer links, wherein each of the second plurality of transfer links specifies a transfer node of the second linked list and a transfer of data between the data acquisition device and the host computer system; and

the host computer system transferring the second plurality of transfer links to the link buffer of the data acquisition device over the communication medium.

37. (New) The method of claim 36,

wherein at least a portion of said executing the plurality of transfer links from the link buffer to transfer data between the data buffer in the data acquisition device and the physical memory of the host computer system and at least a portion of said transferring the second plurality of transfer links to the link buffer of the data acquisition device over the communication medium are performed concurrently.

38. (New) The method of claim 36,

wherein, for each transfer node of the second linked list of transfer nodes, the true address of the transfer node corresponds to a virtual address of a buffer, wherein the buffer spans contiguous virtual addresses mapping to the physical memory of the host computer system, wherein an Mth transfer node corresponds to an Mth virtual address of the buffer.

39. (New) The method of claim 36,

wherein said transferring the plurality of transfer links to the link buffer of the data acquisition device over the communication medium comprises transferring the plurality of transfer links to a first portion of the link buffer of the data acquisition device; and

wherein said transferring the second plurality of transfer links to the link buffer of the data acquisition device over the communication medium comprises transferring the second plurality of transfer links to a second portion of the link buffer of the data acquisition device;

the method further comprising:

the data acquisition device executing the second plurality of transfer links from the second portion of the link buffer to transfer data between the data buffer in the data acquisition device and the physical memory of the host computer system;

the host computer system preparing a third linked list of transfer nodes, wherein each of the third linked list of transfer nodes includes a true address of the physical memory of the host computer system;

the host computer system preparing a third plurality of transfer links, wherein each of the third plurality of transfer links specifies a transfer node of the third linked list and a transfer of data between the data acquisition device and the host computer system; and

the host computer system transferring the third plurality of transfer links to the first portion of the link buffer of the data acquisition device over the communication medium.

40. (New) The method of claim 39,

wherein at least a portion of said executing the second plurality of transfer links from the second portion of the link buffer to transfer data between the data buffer in the data acquisition device and the physical memory of the host computer system and at least a portion of said transferring the third plurality of transfer links to the first portion of the link buffer of the data acquisition device over the communication medium are performed concurrently.

41. (New) The method of claim 39,

wherein, for each transfer node of the third linked list of transfer nodes, the true address of the transfer node corresponds to a virtual address of a buffer, wherein the buffer spans contiguous virtual addresses mapping to the physical memory of the host computer system, wherein a Pth transfer node corresponds to a Pth virtual address of the buffer.

42. (New) The method of claim 39,

wherein the data acquisition device alternates between executing all transfer links from the first portion of the link buffer and all transfer links from the second portion of the link buffer, while the host computer system alternates between transferring transfer links from the host computer system to the second portion of the link buffer and transferring transfer links from the host computer system to the first portion of the link buffer, until there are no more transfer links to transfer from the host computer system.

43. (New) The method of claim 42,

wherein each transfer link comprises at least one of a source address or a destination address, a count of a number of bytes in the transfer, and a pointer to a subsequent transfer link.

44. (New) The method of claim 42,

wherein one or more of the of transfer links comprises a self configuration link, wherein the self configuration link comprises one or more instructions to move data to, from, or between DMA Controller registers of a DMA Controller.

45. (New) The method of claim 44,

wherein the self configuration link is inserted at the end of the plurality of transfer links;

wherein the DMA Controller executes the plurality of transfer links on a DMA channel; and

wherein if the DMA channel reaches the self configuration link before the host computer system has finished transferring the second plurality of transfer links to the second portion of the link buffer, the self configuration link stopping the DMA channel to prevent data overruns.

46. (New) The method of claim 44,

wherein the self configuration link is inserted at the end of the second plurality of transfer links;

wherein the DMA Controller executes the second plurality of transfer links on a DMA channel; and

wherein if the DMA channel reaches the self configuration link before the host computer system has finished transferring the third plurality of transfer links to the first portion of the link buffer, the self configuration link will stop the DMA channel to prevent data overruns.

47. (New) The method of claim 44,

wherein the self configuration link is inserted in the plurality of transfer links; and

wherein the DMA Controller executes the plurality of transfer links on a DMA channel;

when the DMA channel reaches the self configuration link, notifying the host computer system to begin transferring the second plurality of transfer links to the second portion of the link buffer.

48. (New) The method of claim 44,

wherein the self configuration link is inserted in the second plurality of transfer links; and

wherein the DMA Controller executes the second plurality of transfer links on a DMA channel;

the method further comprising:

when the DMA channel reaches the self configuration link, notifying the host computer system to begin transferring the third plurality of transfer links to the first portion of the link buffer.

49. (New) The method of claim 32,

wherein the communication medium comprises an IEEE 1394 bus, which is compliant with an IEEE 1394 protocol specification.

50. (New) The method of claim 49,

wherein the data acquisition device comprises a PCI device; and

wherein the data acquisition device further comprises a PCI/1394 translator;

the method further comprising:

the PCI/1394 translator translating messages between the IEEE 1394 protocol and PCI, thereby providing a mechanism for communication between the IEEE 1394 bus and the PCI device.